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VIGUSHIN, JOHN B	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application No.	Applicant(s)	
	10/072,684	DEVEY, WILLIAM JOHN	
	Examiner	Art Unit	
	John B. Vigushin	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 October 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-9,11-15,17-21 and 23-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *5,12,24 and 32-34* is/are allowed.

6)☒ Claim(s) *1,2,4,6-9,11,13-15,17-21,23,25-31 and 35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The present Office Action is responsive to Applicant's amended Response filed October 03, 2003. The Examiner acknowledges the amendments to Claims 5, 12, 15 and 24, the cancellation of Claims 3, 10, 16 and 22, and the addition of Claims 32-35. Accordingly, Claims 1, 2, 4-9, 11-15, 17-21 and 23-35 are now pending in the instant amended Application.

Claim Objections

2. Claim 35 is objected to because of the following informalities:

In Claim 35, line 10: "devise" should be changed to --devices--.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 15 and 17-19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The "amendment" of Claim 15, although indicated as "amended" in line 6, appears to have been no more than an *attempt* to amend the claim in the wrong place which was evidently recognized by the Applicant as incorrect, whereupon the original recitation "active devices on" was restored in line 6 (please compare "currently

amended" Claim 15 with the originally presented Claim 15). However, the specific defect in the claim that was pointed out on p.2, section 2 in the previous Office Action of July 03, 2003 (Paper No. 0603) was neither corrected or addressed by the Applicant and therefore Claim 15 still recites the defective limitation "said conductive plates of said I/C chip structure" in lines 10-11. There is insufficient antecedent basis for this limitation in the claim. As indicated in the above-cited previous Office Action, the conductive plates belong to the capacitor; not to the IC chip. Again, as indicated in the above-cited previous Office Action, the rejection may be overcome by replacing "conductive plates of" with --active devices on-- in line 10 of "currently amended" Claim 15.

Claims 17-19 depend from Claim 15 and therefore inherit the defect of the claim.

Rejections Based On Prior Art

5. The following references were relied upon for the rejections hereinbelow:

Li (US 2002/0195700 A1)*† Mosley (US 2002/0071258 A1)†

Li et al. (US 6,559,484 B1)**†

*Hereinafter referred to as Li (A1).

**Hereinafter referred to as Li et al. (B1)

† denotes references already made of record in the instant Application.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 2, 4, 6-9, 11, 13, 14, 20, 21, 23, 25 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mosley in view of Li (A1).

A) As to Claim 1:

I. Mosley discloses, in Figs. 1A and 5, and p.3: [0025]: PCB 506 having first and second opposite faces and vias 510 extending from each of the faces; an IC chip structure 515 with at least one active device thereon (typically, a die such as die 303 of Fig. 3; p.2: lines 3-6 of [0023]); connectors 512 connecting the active devices of IC chip structure 515 to vias 510 on one face of PCB 506; decoupling capacitor 503 (Fig. 1A) comprising: at least two interlaced conductive plates (plates 103 and 104 interlaced with plates 105 and 106; pp.1-2: lines 3-6 of [0018]) in dielectric material 113 (pp.1-2: line 16 of [0018]) forming at least one capacitor 100 (in Fig. 1A) or 503 (in Fig. 5); vias 115-118 extending from each of plates 103-106 through dielectric material 113 to connect each via 115-118 to a circuit board via 510 on the second face of PCB 506; vias 115-118 in decoupling capacitor (100 in Fig. 1A or 503 in Fig. 5) being parallel to each other (Fig. 1A) and each via 115-118 connected to one of conductive plates 103-106 being located adjacent a via 115-118 connected to another of conductive plates 103-106 (Fig. 1A).

II. Mosley discloses, in the embodiment of Fig. 2, at least two voltage planes 227 and 230 in PCB 209 (p.2: all of [0022], *especially the last seven lines of the paragraph wherein the capacitor 100 is disclosed as a decoupling capacitor that decouples the PCB-connected power supply for microprocessors, not shown in Fig. 2, that are also*

connected to PCB 209; and therefore, the two metallization layers 227 and 230 are inherently two voltage planes: i.e., a ground/power pair of voltage planes to which the capacitor 100 is necessarily connected in order to perform the disclosed decoupling of the power supply connections for the microprocessors) and vias extending from a face of PCB 209 to the voltage planes 227 and 230 to which the capacitor 100 is connected (Fig. 2) but does not show such voltage planes in the PCB 506 of the embodiment in Fig. 5. However, Mosley does positively disclose that capacitor 503, attached to PCB 506, functions as a decoupling capacitor (p.3: the last five lines of [0025]), as does the capacitor 100 of the Fig. 2 embodiment described above.

III. Li (A1) discloses, in Fig. 5, capacitors 506 mounted to a PCB 502 having an IC chip 508 mounted thereon, first and second opposite faces and vias extending from each of the faces to one of at least two voltage planes 512 and 514 in the PCB 502 which function as power or ground planes for connection to the power and ground pins of the IC chip 508, thus providing the operational power that enables the chip to function, and to which voltage planes capacitor 503 is connected for performing the decoupling of power line noise between the power supply and IC chip 508 (p.3: [0043]).

IV. Since Mosley and Li (A1) are in the same art of fabricating electronic packages with decoupling capacitors, extending the vias of Mosley to power/ground voltage planes to operate the IC chip and capacitor, as taught by Li (A1) and the Fig. 2 embodiment of Mosley would have been readily recognized in the pertinent art of the embodiment of Figs. 1A and 5 in Mosley, and therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to establish at least

two power/ground voltage planes in the PCB 506 of Mosley (Fig. 5) to provide the connections for the power supply, and to extend each of the vias 510 of Mosley (Fig. 5) to one of the power/ground voltage planes in order to provide the IC chip with operational power and provide the capacitor with the power/ground connections to perform the decoupling function, as taught by both Li (A1) and the Fig. 2 embodiment of Mosley.

B) As to Claims 2, 9 and 21:

I. Modified Mosley does not explicitly show the via structure of capacitor 503 but does show the vias 510 in PCB 506 are attached to the circuitry of capacitor 503 in Fig. 5. However, the invention of Mosley is the capacitor 100 shown in Figs. 1A having the arrangement of vias 115-118 suitable for coupling to a substrate, electronic device or a die (see Figs. 1A,B in conjunction with the Fig. 2 embodiment and pp.1-2: last six lines of [0018], wherein the vias 115-118 in capacitor 100 are directly coupled to the vias in substrate 209 that are associated with the voltage planes 227 and 230).

II. Since Mosley desires to minimize parasitic inductance and resistance in the package assembly component-coupling connections (p.1: [0017]) and to reduce the profile (i.e., thickness) of the package (p.2: [0019]), then the coupling connection between PCB 506 and capacitor 503 formed by arranging the PCB vias 510 in the same pattern as the vias in capacitor 506 (capacitor vias not shown in Fig. 5, but shown in Fig. 1A in the capacitor 100 as vias 115-118) would have been readily recognized as providing the same reduction of inductance and package profile in the Fig. 5

embodiment as in the Fig. 2 embodiment, wherein vias 115-118 of capacitor 100 are directly coupled to the corresponding vias in substrate 209.

III. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the embodiment of Fig. 5 of Mosley with the embodiment of Fig. 2, also of Mosley, wherein the vias 510 of PCB 506 are arranged in the same pattern as (i.e., directly coupled to) the corresponding vias in decoupling capacitor 503, as taught in the embodiment of Fig. 2, in order to minimize parasitic inductance and resistance in the connection between the PCB and capacitor and to reduce the package profile, as taught in the Fig. 2 embodiment of Mosley.

C) As to Claims 4, 11 and 23, modified Mosley discloses that vias 510 of PCB 506 and vias 115-118 of capacitor 100 (503), of the Fig. 5 embodiment, are each arranged in a straight line (as evidenced by the capacitor vias in Fig. 1A of Mosley, the vias connecting the voltage planes 227 and 230 to the surface of PCB 209 in the Fig. 2 embodiment of Mosley and the PCB vias 510 in Fig. 5 of Li (A1), the combination of which having already been established in the base Claims 1, 8 and 20 to modify the PCB 506 of the Fig. 5 embodiment in Mosley).

D) As to Claims 6, 13 and 25, modified Mosley discloses that each via 115-118 in decoupling capacitor 100 (503) connected to one via of circuit board 506 (as modified by Li) is completely surrounded by vias in decoupling capacitor 100 connected to another of conductive plates 103-106 (Figs. 1A,B).

E) As to Claims 7, 14 and 26:

I. Modified Mosley does not disclose solder balls provided to decoupling capacitor 503 in Fig. 5 to connect the capacitor to PCB 506 but does evidently teach that pads 133 are used as the interconnection means between capacitor 503 and corresponding chip-receiving pads no PCB 506. However, Mosley further teaches that pads 133 can be used as the above-mentioned interconnection means sites or as a cite for C4 solder balls which also function as an interconnection means; i.e., capacitor 503 can be connected to PCB 506 using C4 solder balls on pads 133 or directly by means of pads 133 (pp.1-2: the last 8 lines of [0018]).

II. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to interconnect capacitor 503 to PCB 506 using the C4 solder balls, as taught by Mosley in the embodiment of Fig 2, since Mosley indicates that the use of C4 solder balls on pad sites 133 and pads 133 are art-recognized equivalent interconnection means which are selected according to the requirements of a particular application.

F) As to Claims 8 and 20:

I. Mosley discloses, in Figs. 1A and 5, and p.3: [0025]: PCB 506 having first and second opposite faces and vias 510 extending from each of the faces; an IC chip structure 515 with at least one active device thereon (typically, a die such as die 303 of Fig. 3; p.2: lines 3-6 of [0023]); connectors 512 connecting the active devices of IC chip structure 515 to vias 510 on one face of PCB 506; a discrete decoupling capacitor 503 (Fig. 1A) comprising: at least two interlaced conductive plates (plates 103 and 104 interlaced with plates 105 and 106; pp.1-2: lines 3-6 of [0018]) in dielectric material 113

(pp.1-2: line 16 of [0018]) forming at least one capacitor 100 (in Fig. 1A) or 503 (in Fig. 5) connected to the other face of PCB 506; vias 115-118 extending from each of plates 103-106 through dielectric material 113 to connect each via 115-118 to a circuit board via 510 on the second face of PCB 506; vias 115-118 in decoupling capacitor (100 in Fig. 1A or 503 in Fig. 5) being parallel to each other (Fig. 1A) and each via 115-118 connected to one of conductive plates 103-106 being located adjacent a via 115-118 connected to another of conductive plates 103-106 (Fig. 1A).

II. Mosley discloses, in the embodiment of Fig. 2, at least two voltage planes 227 and 230 in PCB 209 (p.2: all of [0022], *especially the last seven lines of the paragraph wherein the capacitor 100 is disclosed as a decoupling capacitor that decouples the PCB-connected power supply for microprocessors, not shown in Fig. 2, that are also connected to PCB 209; and therefore, the two metallization layers 227 and 230 are inherently two voltage planes: i.e., a ground/power pair of voltage planes to which the capacitor 100 is necessarily connected in order to perform the disclosed decoupling of the power supply connections for the microprocessors*) and vias extending from a face of PCB 209 to the voltage planes 227 and 230 to which the capacitor 100 is connected (Fig. 2) but does not show such voltage planes in the PCB 506 of the embodiment in Fig. 5. However, Mosley does positively disclose that capacitor 503, attached to PCB 506, functions as a decoupling capacitor (p.3: the last five lines of [0025]), as does the capacitor 100 of the Fig. 2 embodiment described above.

III. Li (A1) discloses, in Fig. 5, capacitors 506 mounted to a PCB 502 having an IC chip 508 mounted thereon, first and second opposite faces and vias extending from

each of the faces to one of at least two voltage planes 512 and 514 in the PCB 502 which function as power or ground planes for connection to the power and ground pins of the IC chip 508, thus providing the operational power that enables the chip to function, and to which voltage planes capacitor 503 is connected for performing the decoupling of power line noise between the power supply and IC chip 508 (p.3: [0043]).

IV. Since Mosley and Li (A1) are in the same art of fabricating electronic packages with decoupling capacitors, extending the vias of Mosley to power/ground voltage planes to operate the IC chip and capacitor, as taught by Li (A1) and the Fig. 2 embodiment of Mosley would have been readily recognized in the pertinent art of the embodiment of Figs. 1A and 5 in Mosley, and therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to establish at least two power/ground voltage planes in the PCB 506 of Mosley (Fig. 5) to provide the connections for the power supply, and to extend each of the vias 510 of Mosley (Fig. 5) to one of the power/ground voltage planes in order to provide the IC chip with operational power and provide the capacitor with the power/ground connections to perform the decoupling function, as taught by both Li (A1) and the Fig. 2 embodiment of Mosley.

8. Claims 15, 17-19 and 27-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Li et al. (B1) in view of Li (A1) and Mosley.

A) As to Claims 15 and 27:

I. Li et al. (B1) discloses, in Fig. 6: a PCB 630 having first and second opposite faces; an IC chip structure 620 having first and second faces and at least one active

device thereon, connectors 625 connecting active devices on IC chip structure 620 through the first face of IC chip structure 620 to PCB 630; a discrete decoupling capacitor 610 connected to IC chip structure 620 through second face of IC chip structure 620.

II. Li et al. (B1) does not disclose: 1) vias and at least two voltage planes in PCB 630, wherein the vias extend from a PCB face to one of the voltage planes and the IC chip connectors 625 connect the active devices to the PCB vias on one face of the PCB 630; 2) a discrete decoupling capacitor structure comprising at least two interlaced conductive planes in dielectric material forming at least one capacitor connected to the active devices on IC chip structure 620; 3) vias extending from each of the conductive plates through the dielectric material to connect each via to a connector on the second face of IC chip structure 620; 4) the vias in decoupling capacitor 610 configured and arranged such that the vias are parallel to each other, and each via connected to one conductive plate is located adjacent a via connected to another conductive plate.

III. With respect to enumerated limitation 1) in section II, above: Li (A1) discloses, in Fig. 5, vias 510 and power/ground voltage planes 512, 514 in PCB 502, wherein the vias extend from a PCB face to one of the voltage planes 512, 514 and the connectors (balls) of IC chip 508 connect the active devices to the PCB vias 510, thus enabling operational power/ground connections to chip 508 (p.3: [0043]).

IV. With respect to enumerated limitations 2), 3) and 4) in section II, above: Mosley discloses, in Figs. 1A and 2: a discrete decoupling capacitor 100 in Fig. 5) structure comprising at least two interlaced conductive plates 103-106 in dielectric

material 113 forming at least one capacitor connected to the active devices on IC chip structure 206 (Fig. 2; p.2: lines 3-6 of [0022]) for performing power noise decoupling for the IC chip 206 as well as other components, such as microprocessors, mounted on PCB 209 (p.2: [0022]); vias 115-118 extending from each of the conductive plates 103-106 through the dielectric material 113 to connect each via 115-118 to a connector 218 on the second face of IC chip structure 206 (Fig. 2); the vias in decoupling capacitor 100 configured and arranged such that the vias 115-118 are parallel to each other, and each via 115-118 connected to one conductive plate 103-106 is located adjacent a via 115-118 connected to another conductive plate 103-106 (Fig. 1A).

V. Since Li et al. (B1) is in the same art of mounting decoupling capacitors to electronic packages as Li (A1) and Mosley, and both Li (A1) and Mosley have similarly structured package PCBs and components mounted thereon, then the power planes and via structure in the PCB of Li (A1), including the connections of the PCB to the IC chip mounted thereon, and the via and interlaced conductive plate structure in the decoupling capacitor of Mosley including the connections of the capacitor to the chip, would have been readily recognized in the pertinent art of Li et al. (B1) in order to establish the interconnections between capacitor, IC chip structure and PCB, thereby providing signal and power connections for package operation; i.e., providing signals and operational power to the IC chip and providing power/ground connections to the capacitor for enabling the capacitor to perform the power noise decoupling, as taught by Li (A1) and Mosley.

VI. Therefore, it would have obvious to one of ordinary skill in the art at the time the invention was made to include the above-cited structures of Li (A1) and Mosley in the PCB, IC chip and decoupling capacitor of Li et al. (B1) in order to establish the required operational connections between the PCB, IC chip and decoupling capacitor in the package of Li et al. (B1), as taught by Li (A1) and Mosley.

B) As to Claim 28:

I. Li et al. (B1) does not disclose that the IC chip structure 620 has vias therein arranged in the same pattern as the pattern of the vias in the decoupling capacitor 610, and each of the vias arranged in the pattern of IC chip structure 620 being connected to active devices of the IC chip structure.

II. With respect to enumerated limitation 5) in section II of the rejection of Claim 27, above: Mosley discloses that the structure of IC chip 206 in Mosley (Fig. 2) has vias therein (i.e., see the vias connecting the active surface of chip 206 to metallization layers 221 and 224 in Fig. 2 of Mosley) arranged in the same pattern as that of the vias 115-118 of capacitor 100 connected to corresponding vias of IC chip 206 (Figs. 1A and 2), and each of the vias arranged in the IC chip structure 206 being connected to the active devices (recall that the element 206 is disclosed by Mosley as either a PCB or **a die**; p.2: lines 3-6 of [0022]).

III. Since both Li et al. (B1) and Mosley are both in the same packaging art and disclose similar package assemblies including decoupling capacitors for IC chips, then structuring the capacitor 610 of Li et al. (B1) to have the arrangement of capacitor 100 of Mosley in Figs. 1A and 2 for the purpose of providing a smaller capacitor that reduces

package size and parasitic inductances (see Mosley, p.1: [0017] and p.2: [0019]), and providing a corresponding via structure in IC chip 620 of Li et al. (B1), as in IC chip 206 of Mosley (Fig. 2) in order to connect the capacitor 610 to the IC chip 620 so that the shortest possible signal path is provided for ensuring the desired reduction in parasitic inductances, as indicated in Mosley, p.1: [0017]), would have been readily recognized in the pertinent art of Li et al. (B1) wherein such reduction in parasitic inductances and package size would be recognized as consistent with the industry-recognized trend towards smaller devices with increased performance reliability.

IV. Therefore, it would have been obvious to one or ordinary skill in the art at the time the invention was made to modify the decoupling capacitor structure 610 and IC structure 620 of Li et al. (B1) in the Fig. 6 embodiment of Li et al. (B1) such that the IC chip structure 620 has vias therein arranged in the same pattern as the pattern of vias in the decoupling capacitor 610, and each of the vias arranged in the pattern in the IC chip structure 620 being connected to the active devices of IC chip structure 620, as taught by Mosley, in order to achieve the industry-recognized objective of smaller devices with increased performance reliability, as taught by Mosley.

C) As to Claims 17 and 29, Li et al. (B1) in Fig. 6, as modified by Li (A1) and Mosley, discloses that vias in decoupling capacitor 610 (see vias 115-118 in decoupling capacitor 100 of Mosley in Fig. 1A) and the vias in the IC chip structure 620 (see the vias in the IC chip structure 206 of Mosley in Fig. 2) are each arranged in a straight line.

D) As to Claims 18 and 30, Li et al. (B1) in Fig. 6, as modified by Li (A1) and Mosley, discloses that each via in decoupling capacitor 610 connected to one via in

PCB 630 is completely surrounded by vias in the capacitor 610 connected to another conductive plate (see vias 115-118 and conductive plates 103-106 of Mosley in Fig. 1A).

E) As to Claims 19 and 31, Li et al. (B1) discloses, in Fig. 6, that solder balls 615 are provided connecting decoupling capacitor 610 to IC chip structure 620.

9. Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Li et al. (B1) in view of Li (A1) and Mosley.

I. Li et al. (B1) discloses, in Fig. 6: a PCB 630 having first and second opposite faces; an IC chip structure 620 having first and second faces and at least one active device thereon, connectors 625 connecting active devices on IC chip structure 620 through the first face of IC chip structure 620 to PCB 630; a discrete decoupling capacitor 610 connected to IC chip structure 620 through second face of IC chip structure 620.

II. Li et al. (B1) does not disclose: 1) vias and at least two voltage planes in PCB 630, wherein the vias extend from a PCB face to one of the voltage planes and the IC chip connectors 625 connect the active devices to the PCB vias on one face of the PCB 630; 2) a discrete decoupling capacitor structure comprising at least two interlaced conductive planes in dielectric material forming at least one capacitor connected to the active devices on IC chip structure 620; 3) vias extending from each of the conductive plates through the dielectric material to connect each via to a connector on the second face of IC chip structure 620; 4) the vias in decoupling capacitor 610 configured and arranged such that the vias are parallel to each other, and each via connected to one

conductive plate is located adjacent a via connected to another conductive plate; 5) the IC chip structure 620 has vias therein arranged in the same pattern as the pattern of the vias in the decoupling capacitor 610 and each of the vias arranged in the pattern of IC chip structure 620 being connected to active devices.

IIIa. With respect to enumerated limitation 1) in section II, above: Li (A1) discloses, in Fig. 5, vias 510 and power/ground voltage planes 512, 514 in PCB 502, wherein the vias extend from a PCB face to one of the voltage planes 512, 514 and the connectors (balls) of IC chip 508 connect the active devices to the PCB vias 510, thus enabling operational power/ground connections to chip 508 (p.3: [0043]).

IIIb. With respect to enumerated limitations 2), 3) and 4) in section II, above: Mosley discloses, in Figs. 1A and 2: a discrete decoupling capacitor 100 in Fig. 5) structure comprising at least two interlaced conductive plates 103-106 in dielectric material 113 forming at least one capacitor connected to the active devices on IC chip structure 206 (Fig. 2; p.2: lines 3-6 of [0022]) for performing power noise decoupling for the IC chip 206 as well as other components, such as microprocessors, mounted on PCB 209 (p.2: [0022]); vias 115-118 extending from each of the conductive plates 103-106 through the dielectric material 113 to connect each via 115-118 to a connector 218 on the second face of IC chip structure 206 (Fig. 2); the vias in decoupling capacitor 100 configured and arranged such that the vias 115-118 are parallel to each other, and each via 115-118 connected to one conductive plate 103-106 is located adjacent a via 115-118 connected to another conductive plate 103-106 (Fig. 1A).

IIIc. Since Li et al. (B1) is in the same art of mounting decoupling capacitors to electronic packages as Li (A1) and Mosley, and both Li (A1) and Mosley have similarly structured package PCBs and components mounted thereon, then the power planes and via structure in the PCB of Li (A1), including the connections of the PCB to the IC chip mounted thereon, and the via and interlaced conductive plate structure in the decoupling capacitor of Mosley including the connections of the capacitor to the chip, would have been readily recognized in the pertinent art of Li et al. (B1) in order to establish the interconnections between capacitor, IC chip structure and PCB, thereby providing signal and power connections for package operation; i.e., providing signals and operational power to the IC chip and providing power/ground connections to the capacitor for enabling the capacitor to perform the power noise decoupling, as taught by Li (A1) and Mosley.

IIId. Therefore, it would have obvious to one of ordinary skill in the art at the time the invention was made to include the above-cited structures of Li (A1) and Mosley in the PCB, IC chip and decoupling capacitor of Li et al. (B1) in order to establish the required operational connections between the PCB, IC chip and decoupling capacitor in the package of Li et al. (B1), as taught by Li (A1) and Mosley.

IVa. With respect to enumerated limitation 5) in section II, above: Mosley discloses that the structure of IC chip 206 in Mosley (Fig. 2) has vias therein (i.e., see the vias connecting the active surface of chip 206 to metallization layers 221 and 224 in Fig. 2 of Mosley) arranged in the same pattern as that of the vias 115-118 of capacitor 100 connected to corresponding vias of IC chip 206 (Figs. 1A and 2), and each of the

vias arranged in the IC chip structure 206 being connected to the active devices (recall that the element 206 is disclosed by Mosley as either a PCB or **a die**; p.2: lines 3-6 of [0022]).

IVb. Since both Li et al. (B1) and Mosley are both in the same packaging art and disclose similar package assemblies including decoupling capacitors for IC chips, then structuring the capacitor 610 of Li et al. (B1) to have the arrangement of capacitor 100 of Mosley in Figs. 1A and 2 for the purpose of providing a smaller capacitor that reduces package size and parasitic inductances (see Mosley, p.1: [0017] and p.2: [0019]), and providing a corresponding via structure in IC chip 620 of Li et al. (B1), as in IC chip 206 of Mosley (Fig. 2) in order to connect the capacitor 610 to the IC chip 620 so that the shortest possible signal path is provided for ensuring the desired reduction in parasitic inductances, as indicated in Mosley, p.1: [0017]), would have been readily recognized in the pertinent art of Li et al. (B1) wherein such reduction in parasitic inductances and package size would be recognized as consistent with the industry-recognized trend towards smaller devices with increased performance reliability.

IVc. Therefore, it would have been obvious to one or ordinary skill in the art at the time the invention was made to modify the decoupling capacitor structure 610 and IC structure 620 of Li et al. (B1) in the Fig. 6 embodiment of Li et al. (B1) such that the IC chip structure 620 has vias therein arranged in the same pattern as the pattern of vias in the decoupling capacitor 610, and each of the vias arranged in the pattern in the IC chip structure 620 being connected to the active devices of IC chip structure 620, as taught

by Mosley, in order to achieve the industry-recognized objective of smaller devices with increased performance reliability, as taught by Mosley.

Allowable Subject Matter

10. Claims 32 and 5, 33 and 12, 34 and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. The following is a statement of reasons for the indication of allowable subject matter:

As to Claims 32 and 5, 33 and 12, 34 and 24, patentability resides in the limitation wherein *the IC chip structure has vias therein arranged in the same pattern as the pattern of the vias in the decoupling capacitor*, in combination with the other limitations of base Claims 32, 33 and 34, respectively.

12. As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

Response to Arguments

13. Applicant's arguments filed October 03, 2003 have been fully considered but they are not persuasive.

14. The Examiner acknowledges the Applicant's correct observation that all the prior art rejections in the previous Office Action of July 03, 2003 were in fact 35 USC § 103(a)

rejections that were placed under the captions of 35 USC § 102(e) by mistake. The Examiner regrets the error and any confusion it may have caused. In the present Office Action, the Examiner has repeated the rejections of the previous Office Action and corrected the captions; i.e., changed them to 35 USC § 103(a) captions, as originally intended. Some of the rejections have been revised only to the extent of further clarifying the Examiner's already-stated positions from the previous Office Action, thus making more apparent the nexus between the combined references, or, between different embodiments within a reference, and the motivations to so combine.

15. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). The Examiner takes the position that the nexus between the combined references, or between different embodiments within a reference, has been thoroughly set forth and that the motivations to combine the references, or different embodiments within a reference, have been clearly justified in the present Office Action, just as in the previous Office Action. The Examiner has therefore maintained his rejections of the originally presented subject matter in Claims 1, 2, 4, 6-9, 11, 13-15, 17-21, 23, 25, 26-31 and the new independent Claim 35 (which comprises the subject matter of canceled Claim 16, now written as the independent claim).

16. As indicated above, in section 4 of the present Office Action, the attempt by the Applicant to correct the 35 USC § 112, 2nd paragraph defect in Claim 15 was

unsuccessful and therefore, the Examiner has repeated the rejection. An additional minor informality was detected in new Claim 35 and objected to in section 2, above.

Conclusion

17. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 703-308-1205 (Crystal City campus) or 571-272-1936 (Carlyle campus). The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 703-308-1233 (Crystal City campus) or 571-272-1957 (Carlyle campus). The fax phone number for the organization where this application or proceeding is assigned is 703-308-7382.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

John B. Vigushin
Primary Examiner
Art Unit 2827

jbv
January 04, 2004